FERROELECTRIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF REDUCING OPERATION FREQUENCEY OF REFERENCE CELL

Field of the Invention

The present invention relates to a semiconductor device; and, more particularly, to a ferroelectric random access memory (FeRAM) device capable of reducing operation frequency of a reference cell.

Description of the Prior Art

Generally, a ferroelectric random access memory (FeRAM) device is a non-volatile semiconductor memory device, which employs the characteristics of a ferroelectric material having the residual polarity of a negative or positive direction. A structure of the ferroelectric random access memory is similar to that of a dynamic random access memory (DRAM) except that a storage element is made of the ferroelectric material.

In the FeRAM, there have been two conventional schemes in order to discriminate whether data written to a memory cell is "0" or "1". The first conventional scheme employs a plurality of memory cells arranged in a matrix, each of which includes two transistors and two ferroelectric capacitors. The data discrimination of the first conventional scheme is accomplished by using the two ferroelectric capacitors, which are connected to a pair of bit lines, e.g. a bit line and a bit line bar, wherein one ferroelectric capacitor is connected to the bit line and the other ferroelectric

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capacitor is connected to the bit line bar. That is, a "1" is written to one ferroelectric capacitor and a "0" is written to the other ferroelectric capacitor.

On the other hand, a second conventional scheme employs a plurality of memory cells arranged in a matrix, each of which includes one transistor and one ferroelectric capacitor, while one column of the memory cells is provided with one reference cell having a storage element, i.e. a ferroelectric capacitor. To discriminate whether data written to a memory cell is "0" or "1", the reference cell has the average of electric charges applied to a bit line. Accordingly, the data discrimination of the second conventional scheme is accomplished by using the reference cell, which discharges the average electric charges.

The second conventional scheme may reduce a cell area more than the first conventional scheme. However, every time each memory cell contained in the same column is selected, the corresponding reference cells should be also selected. Therefore, since operation frequency of the reference cell is greater than that of each memory cell contained in the same column, the ferroelectric capacitors of the corresponding reference cell are fatigued faster than the ferroelectric capacitor of each memory cell contained in the same column. As a result, the life span of the ferroelectric capacitor of the reference cell can be severely reduced, thereby affecting the reliance of the FeRAM.

Summary of the Invention

It is, therefore, an object of the present invention to provide a ferroelectric random access memory (FeRAM) that reduces operation frequency of a reference cell, thereby reducing the fatigue of a ferroelectric capacitor of the reference cell.

In accordance with an aspect of the present invention, there is provided a ferroelectric random access memory (FeRAM) device, comprising: a plurality of memory cells arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer; a number of reference cells connected to each column of the memory cells; and a cell selection means for selecting a memory cell in response to address signals from an external circuit and selecting a reference cell corresponding to the selected memory cell.

Brief Description of the Drawings

Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing memory cells and reference cells of a ferroelectric random access memory device in accordance with the present invention; and

Fig. 2 is a circuit diagram showing a memory cell selection circuit and a reference cell selection circuit connected to Fig. 1.

Detailed Description of the Invention

Referring to Fig. 1, a ferroelectric random access memory (FeRAM) device in accordance with the present invention includes a plurality of memory cells 10 connected to a bit line BL0 and a number of reference cells 20 connected to a bit line BL1 adjacent to the bit line BL0. The memory cells 10 is arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer. If the number of memory cells of each column is $M = 2^N$, the number of reference cells is N. For example, if the number of the memory cells is 2^8, the number of the reference cells is eight. The N number of reference cells 20 connected to each column of the memory cells 10. For the sake of convenience, an M × 1 matrix of memory cells is shown in Fig. 1.

Also, a cell plate CP0 is positioned between the bit line BL0 and the bit line BL1. The memory cells 10, each of which includes one transistor and one ferroelectric capacitor. Similarly, the reference cells 20, each of which includes one transistor and one ferroelectric capacitor. When one of word lines (WL0 to WLM-1) is selected to operate one of the memory cells 10, a ferroelectric capacitor of the memory cell 10 operated discharges electric charges to the bit line BL0. When one of reference word lines (RWL0 to RWLN-1) is selected to operate one of reference cells 20, a ferroelectric capacitor of the reference cell 20 operated discharges electric charges to the bit line BL1.

Accordingly, the data discrimination is accomplished by

comparing the electric charges of the reference cell 20 with that of the memory cell 10. At this time, the operation frequency of the reference cells 20 is reduced more than that of the conventional reference cell. Thus, the reduction of the magnitude of residual polarity can be delayed in the ferroelectric capacitor of the reference cells 20 and its life span can be increased.

Referring to Fig. 2, the memory cells 10 shown in Fig. 1 are connected to a memory cell selection circuit 200 and the reference cells 20 shown in Fig. 1 are connected to a reference cell selection circuit 300.

The memory cell selection circuit 200 includes NAND gates 201 and inverters 202 to generate a memory cell selection signal in response to address signals. Also, the reference cell selection circuit 300 includes NAND gates 301 and inverters 302 to generate a reference cell selection signal to select a corresponding reference cell.

When it is assumed that the memory cell selection circuit 200 is connected to the memory cells 10 via 256 word lines WL0 to WL255, a NAND gate 201 receives eight address signals from an external circuit. The NAND gate 201 performs NAND logical operation, and an inverter 202 inverts an output signal of the NAND gate 201 to generate the memory cell selection signal, wherein the NAND gate 201 has eight input terminals.

The reference cell selection circuit 300 includes NAND gates 301 and inverters 302 to generate a reference cell selection signal. When it is assumed that the reference cell selection circuit 300 is connected to the reference cells via eight reference word lines

RWL0 to RWL7, a NAND gate 301 receives three address signals from the external circuit. The NAND gate 301 performs NAND logical operation and an inverter 302 inverts an output signal of the NAND gate 301 to generate the reference cell selection signal, wherein the NAND gate 301 has three input terminals.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.